FAIRCHILD SEMICONDUCTOR®

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FAN50FC3 — 8-Bit Programmable, 2- to 3-Phase FastvCore™ Buck Controller

Features

- FastvCore™ nonlinear control for fast transient and to minimizes the number of output caps required
- Selectable 2- or 3-phase operation at up to 1MHz per phase
- ±7.7mV worst-case differential sensing error over temperature
- Active current balancing between output phases
- Power Good and Crowbar blanking supports on-the-fly VID code changes
- 0.5V to 1.6V output
- Usable for Intel® VR10 and VR11 designs
- Selectable VR10 extended (7-bit) and VR11 (8-bit) VID tables
- Programmable soft-start ramp
- Programmable short-circuit protection and latch-off delay

Applications

- Desktop PC/Server processor power supplies for existing and next-generation Intel® processors
- VRM modules

Related Applications Notes

- *AN-6052 — Instructions for the Multi-Phase VR11 MathCad® Design Tool*

Description

The FAN50FC3 device is a multi-phase buck switching regulator controller optimized to convert a 12V input supply to the processor core voltage required by high-performance Intel® processors. It has an internal, 8-bit DAC that converts a digital voltage identification (VID) code sent from the processor, to set the output voltage between 0.5V and 1.6V in 6.25mV steps. It outputs PWM signals to external MOSFET drivers that drive the switching power MOSFETs. The switching frequency of the design is programmable by a single resistor value and the number of phases can be programmed to support 2- or 3-phase applications.

The FAN50FC3 also includes programmable no-load offset and droop functions to adjust the output voltage as a function of the load current, as required by the Intel® specifications. The FAN50FC3 also provides an accurate and reliable short-circuit protection function with an adjustable over-current set point.

FastvCore™ technology greatly improves the fast transient response required by today's high-performance processors. This allows fewer output capacitors to be used in the application.

The FAN50FC3 is specified over the commercial temperature range of 0°C to +85°C and is available in a 32-lead MLP package.

Ordering Information

Part Number	Pb-Free	Operating Temperature Range	Package	Packing Method
FAN50FC3MPX	Yes	0 to 85°C	32-Lead, Molded Leadless Package (MLP)	Tape and Reel

Block Diagram

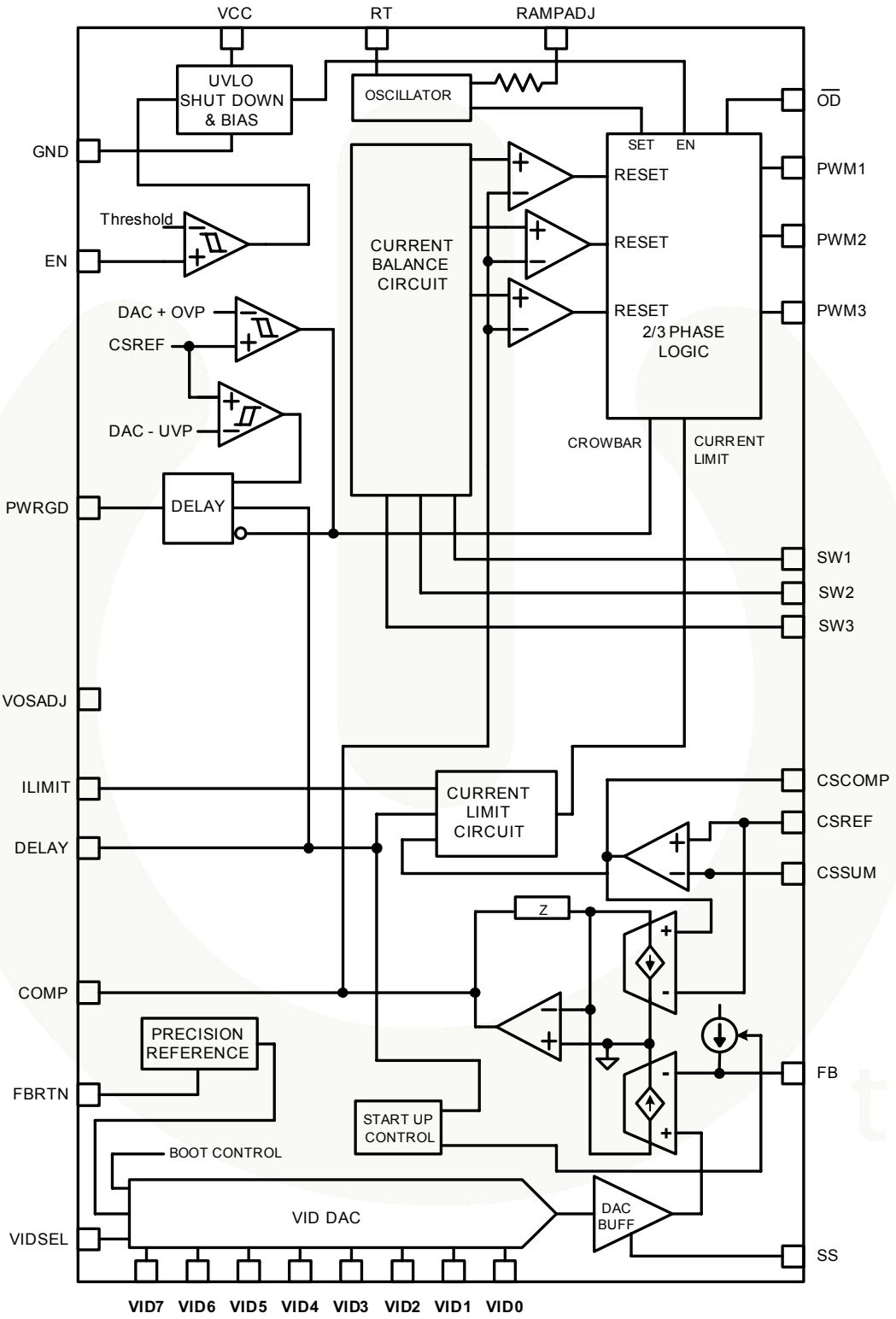


Figure 1. Block Diagram

Pin Assignments

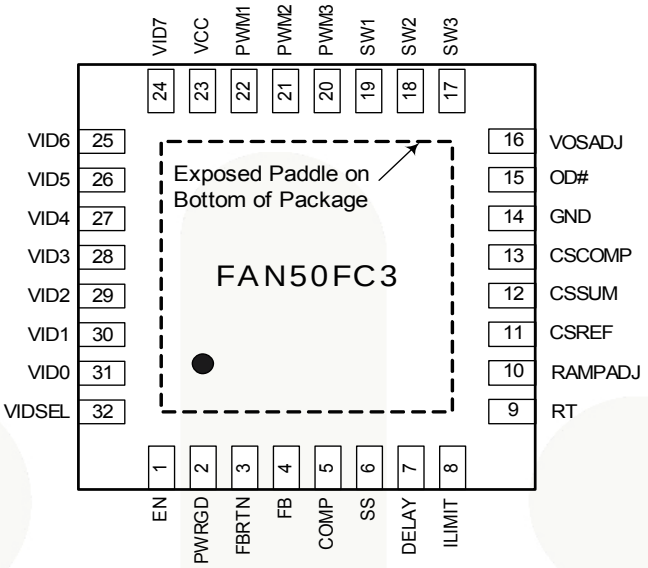


Figure 2. Pin Assignments

Pin Definitions

Pin #	Name	Description
1	EN	**Power Supply Enable Input**. Analog comparator input with hysteresis. If the input voltage is higher than the internal threshold, the controller is enabled; if lower, the controller is disabled.
2	PWRGD	**Power Good Output**. Open-drain output that pulls to GND when the output voltage is outside the proper operating range.
3	FBRTN	**Feedback Return**. VID DAC and error amplifier reference for remote sensing output voltage.
4	FB	**Feedback Input**. Error amplifier input for remote sensing output voltage. A positive internal current source is connected to this pin to allow the output voltage to be offset lower than the DAC voltage.
5	COMP	**Error Amplifier Output**. For loop compensation.
6	SS	**Soft-Start Input**. An external capacitor connected between this pin and GND sets the soft-start ramp-up time.
7	DELAY	**Delay Timer Input**. An external capacitor connected between this pin and GND sets the over-current latch-off delay time, BOOT voltage hold time, EN delay time, and PWRGD delay time.
8	ILIMIT	**Current Limit Set**. An external resistor from this pin to GND sets the current limit threshold of the converter.
9	RT	**Frequency Set Input**. An external resistor connected between this pin and GND sets the oscillator frequency of the device.
10	RAMPADJ	**PWM Ramp Set Input**. An external resistor connected between this pin and the converter input voltage sets the internal PWM ramp.
11	CSREF	**Current-Sense Amplifier Positive Input**. The voltage on this pin is used as the reference for the current-sense amplifier. The Power Good and Crowbar functions are internally connected to this pin.
12	CSSUM	**Current-Sense Amplifier Negative Input**.
13	CSCOMP	**Current-Sense Amplifier Compensation Output**.

Pin Definitions (Continued)

14	GND	**Ground**. Biasing and logic output signals of the device are referenced to this ground.
15	OD#	**Output Disable**. This pin is actively pulled LOW when the EN input is low or when V_{CC} is below the UVLO threshold, to disable the external MOSFET drivers.
16	VOSADJ	**FastvCore™ V_{OS} Adjustment Input.** This signal is used as a control input for the FastvCore™ circuit.
17 to 19	SW3 to SW1	**Switching Node Current Balance Inputs**. Sense the switching side of the inductor and used to measure the current level in each phase. The SW pins of unused phases should be left open.
20 to 22	PWM3 to PWM1	**PWM Outputs**. Each output is connected to the input of an external MOSFET driver, such as the FAN5109. Connecting the PWM3 output to V_{CC} disables that phase, allowing the FAN50FC3 to operate as a 2-phase controller.
23	VCC	**Supply Voltage**.
24 to 31	VID7 to VID0	**Voltage Identification Code Inputs**. These digital inputs are connected to the internal DAC and used to program the output voltage. These pins have 1µA internal pull-down; if they are left open, the input state is decoded as logic LOW.
32	VIDSEL	**VID Table Select Input**. A logic LOW selects the extended VR10 DAC table and a logic HIGH selects the VR11 DAC table. This pin has a 1µA internal pull-down; if left open, the input state is decoded as logic LOW.
	Exposed Paddle	**Internally Connected to Die Ground**. May be connected to ground or left floating. Connect to ground for lowest package thermal resistance.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
	Supply Voltage, VCC	-0.3	+15	V
	FBRTN	-0.3	+0.3	V
	RAMPADJ, PWM3	-0.3	V_{CC} +0.3	V
	SW1 – SW3	-10	+25	V
	All Other Inputs and Outputs	-0.3	+5.5	V
T_J	Operating Junction Temperature	0	+125	°C
T_{STG}	Storage Temperature	-65	+150	°C
T_{LS}	Lead Soldering Temperature (10 Seconds)		300	°C
T_{LI}	Lead Infrared Temperature (15 Seconds)		260	°C
θ_{JA}	Thermal Resistance, Junction-to-Ambient(1)		45	°C/W

Note:

1. Junction-to-ambient thermal resistance, θ_{JA}, is a strong function of PCB material, board thickness, thickness and number of copper planes, number of via used, diameter of via used, available copper surface, and attached heat sink characteristics.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	VCC to GND	9.6	12.0	14.4	V
T_A	Ambient Temperature		0		+85	°C

Electrical Characteristics

V_{CC} = 12V, FBRTN = GND, and T_A = +25°C. The • denotes specifications which apply over the full operating temperature range.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
Error Amplifier							
V_{COMP}	Output Voltage Range		•	0.5		4.0	V
V_{FB}	Accuracy	Relative to nominal DAC output, referenced to FBRTN. *(see Figure 3)*	•	-7.7		+7.7	mV
$V_{FB(BOOT)}$	Accuracy	VRM11 VID Range: 1.00625V to 1.60000V During Start-up	•	1.092	1.100	1.108	V
	Load Line Droop Accuracy	CSREF-CSCOMP= 80mV *(see Figure 5)*	•	-78	-80	-82	mV
	Differential Non-Linearity		•	-1		+1	LSB
ΔV_{FB}	Line Regulation	V_{CC} =10V to 14V			0.05		%
I_{FB}	Input Bias Current		•	13.5	15	16.5	µA
I_{FBRTN}	FBRTN Current		•		70	95	µA
$I_{O(ERR)}$	Output Current	FB forced to V_{OUT} -3%			500		µA
$GBW_{(ERR)}$	Gain Bandwidth Product	COMP = FB[3]			20		MHz
	Slew Rate	COMP = FB[3]			25		V/µs
V_{CSCOMP}	CSCOMP Voltage Range	Relative to CSREF	•	-250		+250	mV
t_{BOOT}	BOOT Voltage Hold Time	C_{DELAY} = 10nF			2		ms
VID Inputs and VIDSEL							
$V_{IL(VID)}$	Input Low Voltage	VIDx, VIDSEL	•			0.4	V
$V_{IH(VID)}$	Input High Voltage	VIDx, VIDSEL	•	0.8		3.3	V
$V_{IL(VID)}$	Select VR10 Table	VIDSEL Logic LOW				0.4	V
$V_{IH(VID)}$	Select VR11 Table	VIDSEL Logic HIGH		0.8		3.3	V
$I_{IN(VID)}$	Input Current, VID Low				-1		µA
$t_{DLY(VID)}$	VID Transition Delay Time	VID code change to FB change[3]	•	200			ns
$t_{DLY(CPU)}$	No CPU Detection Turn-off Delay Time	VID code change to off state to PWM going LOW[3]	•	200			ns
Oscillator							
f_{OSC}	Frequency		•	0.25		4.50	MHz
f_{PHASE}	Frequency Variation	T_A = 25C, R_T= 200K, 3-phase		-20%	400	20%	kHz
V_{RT}	Output Voltage	R_T =100kΩ to GND	•	1.9	2.0	2.1	V
$V_{RAMPADJ}$	RAMPADJ Output Voltage	$V_{RAMPADJ} = V_{DAC} + 2k\Omega * (V_{CC} - V_{DAC}) / (R_{RAMPADJ} + 2K\Omega)$	•	-50		+50	mV
$I_{RAMPADJ}$	RAMPADJ Input Current Range			1		50	µA
Current-Sense Amplifier							
$V_{OS(CSA)}$	Offset Voltage	CSSUM – CSREF *(see Figure 4)*	•	-1.0		+1.0	mV
$I_{BIAS(CSSUM)}$	Input Bias Current (for CSSUM)		•	-50		+50	nA
$I_{BIAS(CSREF)}$	Input Current (for CSREF)	Current drawn by CSREF Pin	•	-3		+3	µA
$GBW_{(CSA)}$	Gain Bandwidth Product	CSSUM = CSCOMP[3]			10		MHz
	Slew Rate	C_{CSCOMP} = 10pF[3]			10		V/µs
V_{CSACM}	Input Common-Mode Range	CSSUM and CSREF	•	0		3.2	V

Electrical Characteristics (Continued)

V_{CC} = 12V, FBRTN = GND, and T_A = +25°C. The • denotes specifications which apply over the full operating temperature range.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
Current-Sense Amplifier (Continued)							
	Output Voltage Range		•	0.05		3.20	V
I_{CSCOMP}	Output Current				1		mA
Current Balance Circuit							
$V_{SW(x)CM}$	Common Mode Range(3)		•	-600		+200	mV
$R_{SW(x)}$	Input Resistance	SW(x) = 0V	•	35	50	65	kΩ
$I_{SW(x)}$	Input Current	SW(x) = 0V	•	1.6	3.3	5.0	µA
$\Delta I_{SW(x)}$	Input Current Matching	SW(x) = 0V	•	-5		+5	%
Current Limit Comparator							
V_{ILIMIT}	Output Voltage	R_{ILIMT} = 143kΩ	•	1.6	1.7	1.8	V
I_{ILIMIT}	Output Current	R_{ILIMT} = 143kΩ			12		µA
	Maximum Output Current		•	60			µA
V_{CL}	Current Limit Threshold Voltage	$V_{CSREF} - V_{CSCOMP}$, R_{ILIMT} = 143kΩ	•	100	120	140	mV
	Current Limit Setting Ratio	V_{CL} / I_{ILIMT}			10		mV/µA
Delay Timer							
I_{DELAY}	Normal Mode Output Current		•	12	15	18	µA
$I_{DELAY(CL)}$	Output Current in Current Limit		•	3.00	3.75	4.50	µA
$V_{DELAY(TH)}$	Threshold Voltage		•	1.6	1.7	1.8	V
Soft-Start							
$I_{(SS)}$	Output Current	During Start-up	•	12	15	18	µA
Enable Input							
$V_{TH(EN)}$	Threshold Voltage		•	800	850	900	mV
$V_{HYS(EN)}$	Threshold Hysteresis		•	80	100	130	mV
$I_{IN(EN)}$	Enable Input Current				1		µA
$t_{DELAY(EN)}$	Turn-On Delay	Start-up sequence, EN>950mV, C_{DELAY} = 10nF			2		ms
#OD Output							
$V_{OL(ODB)}$	Output Voltage LOW	$I_{PWM(SINK)}$ = 400µA	•		160	400	mV
$V_{OH(ODB)}$	Output Voltage HIGH	$I_{PWM(SOURCE)}$ = 400µA	•	4	5		V
Power-Good Comparator							
$V_{PWRGD(UV)}$	Under-Voltage Threshold	Relative to Nominal DAC Output	•	-300	-250	-200	mV
$V_{PWRGD(OV)}$	Over-Voltage Threshold	Relative to Nominal DAC Output	•	100	150	200	mV
$V_{OL(PWRGD)}$	Output Low Voltage	$I_{PWRGD(SINK)}$ = -4mA	•		200	300	mV
$t1_{PG(DLY)}$	Power Good Delay Time 1	Start-up Sequence; C_{DELAY} = 10nF; Power Good Blanking Time	•		2		ms
$t2_{PG(DLY)}$	Power Good Delay Time 2	VID Code Changing; C_{DELAY} = 10nF; Power Good Blanking Time	•	100	250		µs
$t3_{PG(DLY)}$	Power Good Delay Time 3(3)	VID Code Static; C_{DELAY} = 10nF; Power Good Blanking Time	•	100	200		ns

Electrical Characteristics (Continued)

V_{CC} = 12V, FBRTN = GND, and T_A = +25°C. The • denotes specifications which apply over the full operating temperature range.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
Power-Good Comparator (Continued)							
$V_{CROWBAR}$	Crowbar Trip Point	Relative to Nominal DAC Output	•	100	150	200	mV
V_{CR_RST}	Crowbar Reset Point	Relative to FBRTN	•	250	300	350	mV
$t1_{CROWBAR}$	Crowbar Delay Time 1	VID Code Change Over-Voltage to PWM Going LOW Crowbar Blanking Time	•	100	250		µs
$t2_{CROWBAR}$	Crowbar Delay Time 2	VID Code Static Over-Voltage to PWM going LOW Crowbar Blanking Time	•		400		ns
PWM Outputs							
$V_{OL(VRTM)}$	Output Voltage Low	$I_{PWM(SINK)}$ = 400µA	•		160	400	mV
$V_{OH(VRTM)}$	Output Voltage High	$I_{PWM(SOURCE)}$ = 400µA	•	4	5		V
V_{DIS}	Phase Disable Voltage	Applicable to PWM3 pins only. Connect this pin to VCC to disable the phase.(4)	•	V_{CC} -.1			V
Input Supply							
I_{DC}	DC Supply Current	EN = Logic HIGH	•		8	12	mA
V_{UVLO}	UVLO Threshold	V_{CC} Rising	•	6.5	6.9	7.3	V
V_{UVLO_HYS}	UVLO Hysteresis		•	0.7	0.9	1.1	V

Notes:

2. Limits at operating temperature extremes are guaranteed by design, characterization, and statistical quality control.
3. AC specifications are guaranteed by design and characterization; not production tested.
4. To operate the FAN50FC3 with fewer than three phases, PWM3 should be connected to V_{CC} to disable this phase. *See the Theory of Operation section for details.*

Test Diagrams

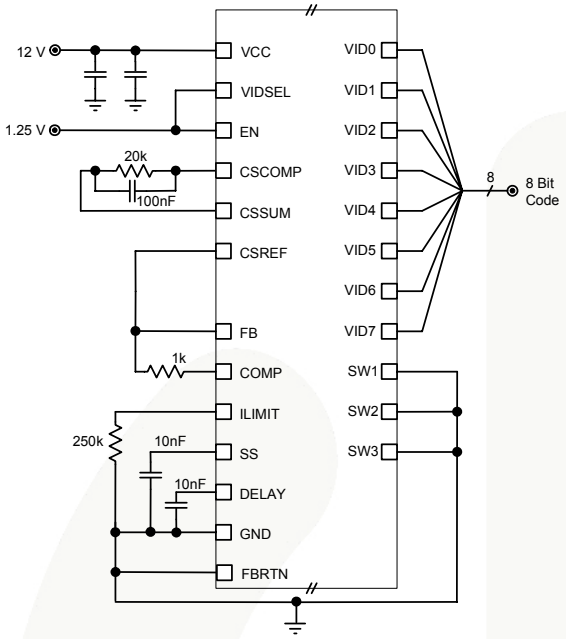


Figure 3. Closed-Loop Output Voltage Accuracy

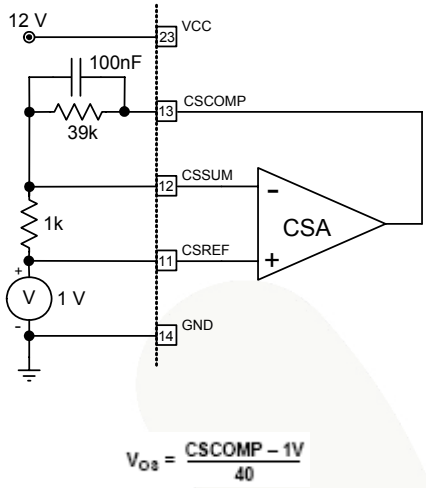


Figure 4. Current-Sense Amplifier V_{OS}

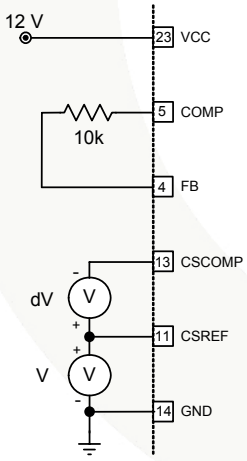


Figure 5. Droop Voltage Accuracy

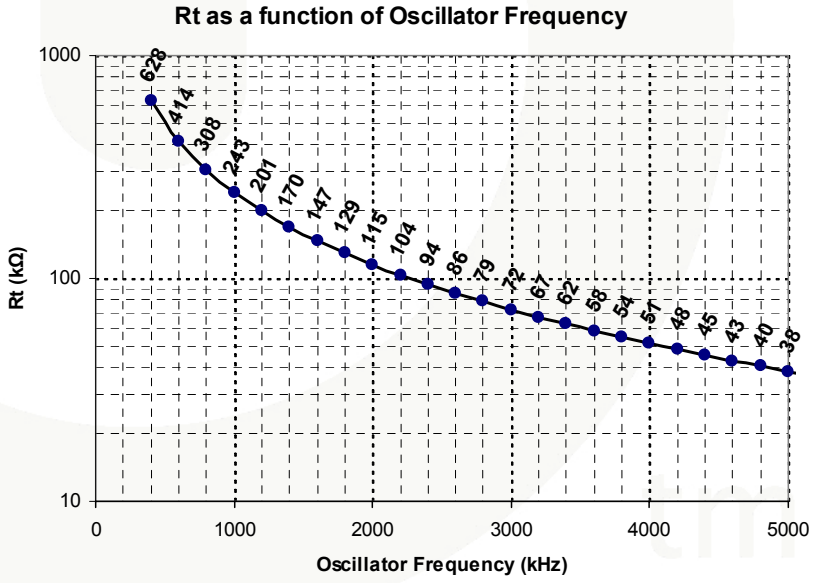


Figure 6. R_T Required to Set Oscillator Frequency

Table 1. Output Voltage Programming Codes (extended VR10); 0 = logic LOW; 1 = logic HIGH.

VID4	VID3	VID2	VID1	VID0	VID5	VID6	V_{OUT} (V)
1	1	1	1	1	1	0	OFF
1	1	1	1	1	1	1	OFF
1	1	1	1	1	0	0	OFF
1	1	1	1	1	0	1	OFF
1	1	1	1	0	1	0	1.09375
1	1	1	1	0	1	1	1.10000
1	1	1	1	0	0	0	1.10625
1	1	1	1	0	0	1	1.11250
1	1	1	0	1	1	0	1.11875
1	1	1	0	1	1	1	1.12500
1	1	1	0	1	0	0	1.13125
1	1	1	0	1	0	1	1.13750
1	1	1	0	0	1	0	1.14375
1	1	1	0	0	1	1	1.15000
1	1	1	0	0	0	0	1.15625
1	1	1	0	0	0	1	1.16250
1	1	0	1	1	1	0	1.16875
1	1	0	1	1	1	1	1.17500
1	1	0	1	1	0	0	1.18125
1	1	0	1	1	0	1	1.18750
1	1	0	1	0	1	0	1.19375
1	1	0	1	0	1	1	1.20000
1	1	0	1	0	0	0	1.20625
1	1	0	1	0	0	1	1.21250
1	1	0	0	1	1	0	1.21875
1	1	0	0	1	1	1	1.22500
1	1	0	0	1	0	0	1.23125
1	1	0	0	1	0	1	1.23750
1	1	0	0	0	1	0	1.24375
1	1	0	0	0	1	1	1.25000
1	1	0	0	0	0	0	1.25625
1	1	0	0	0	0	1	1.26250
1	0	1	1	1	1	0	1.26875
1	0	1	1	1	1	1	1.27500
1	0	1	1	1	0	0	1.28125
1	0	1	1	1	0	1	1.28750
1	0	1	1	0	1	0	1.29375
1	0	1	1	0	1	1	1.30000
1	0	1	1	0	0	0	1.30625
1	0	1	1	0	0	1	1.31250
1	0	1	0	1	1	0	1.31875
1	0	1	0	1	1	1	1.32500
1	0	1	0	1	0	0	1.33125
1	0	1	0	1	0	1	1.33750
1	0	1	0	0	1	0	1.34375
1	0	1	0	0	1	1	1.35000
1	0	1	0	0	0	0	1.35625
1	0	1	0	0	0	1	1.36250
1	0	0	1	1	1	0	1.36875
1	0	0	1	1	1	1	1.37500
1	0	0	1	1	0	0	1.38125
1	0	0	1	1	0	1	1.38750
1	0	0	1	0	1	0	1.39375
1	0	0	1	0	1	1	1.40000
1	0	0	1	0	0	0	1.40625
1	0	0	1	0	0	1	1.41250
1	0	0	0	1	1	0	1.41875
1	0	0	0	1	1	1	1.42500
1	0	0	0	1	0	0	1.43125
1	0	0	0	1	0	1	1.43750
1	0	0	0	0	1	0	1.44375
1	0	0	0	0	1	1	1.45000
1	0	0	0	0	0	0	1.45625
1	0	0	0	0	0	1	1.46250
0	1	1	1	1	1	0	1.46875
0	1	1	1	1	1	1	1.47500

VID4	VID3	VID2	VID1	VID0	VID5	VID6	V_{OUT} (V)
0	1	1	1	1	0	0	1.48125
0	1	1	1	1	0	1	1.48750
0	1	1	1	0	1	0	1.49375
0	1	1	1	0	1	1	1.50000
0	1	1	1	0	0	0	1.50625
0	1	1	1	0	0	1	1.51250
0	1	1	0	1	1	0	1.51875
0	1	1	0	1	1	1	1.52500
0	1	1	0	1	0	0	1.53125
0	1	1	0	1	0	1	1.53750
0	1	1	0	0	1	0	1.54375
0	1	1	0	0	1	1	1.55000
0	1	1	0	0	0	0	1.55625
0	1	1	0	0	0	1	1.56250
0	1	0	1	1	1	0	1.56875
0	1	0	1	1	1	1	1.57500
0	1	0	1	1	0	0	1.58125
0	1	0	1	1	0	1	1.58750
0	1	0	1	0	1	0	1.59375
0	1	0	1	0	1	1	1.60000
0	1	0	1	0	0	0	0.83125
0	1	0	1	0	0	1	0.83750
0	1	0	0	1	1	0	0.84375
0	1	0	0	1	1	1	0.85000
0	1	0	0	1	0	0	0.85625
0	1	0	0	1	0	1	0.86250
0	1	0	0	0	1	0	0.86875
0	1	0	0	0	1	1	0.87500
0	1	0	0	0	0	0	0.88125
0	1	0	0	0	0	1	0.88750
0	0	1	1	1	1	0	0.89375
0	0	1	1	1	1	1	0.90000
0	0	1	1	1	0	0	0.90625
0	0	1	1	1	0	1	0.91250
0	0	1	1	0	1	0	0.91875
0	0	1	1	0	1	1	0.92500
0	0	1	1	0	0	0	0.93125
0	0	1	1	0	0	1	0.93750
0	0	1	0	1	1	0	0.94375
0	0	1	0	1	1	1	0.95000
0	0	1	0	1	0	0	0.95625
0	0	1	0	1	0	1	0.96250
0	0	1	0	0	1	0	0.96875
0	0	1	0	0	1	1	0.97500
0	0	1	0	0	0	0	0.98125
0	0	1	0	0	0	1	0.98750
0	0	0	1	1	1	0	0.99375
0	0	0	1	1	1	1	1.00000
0	0	0	1	1	0	0	1.00625
0	0	0	1	1	0	1	1.01250
0	0	0	1	0	1	0	1.01875
0	0	0	1	0	1	1	1.02500
0	0	0	1	0	0	0	1.03125
0	0	0	1	0	0	1	1.03750
0	0	0	0	1	1	0	1.04375
0	0	0	0	1	1	1	1.05000
0	0	0	0	1	0	0	1.05625
0	0	0	0	1	0	1	1.06250
0	0	0	0	0	1	0	1.06875
0	0	0	0	0	1	1	1.07500
0	0	0	0	0	0	0	1.08125
0	0	0	0	0	0	1	1.08750

Table 2. Output Voltage Programming Codes (8 Bit) 0 = logic LOW; 1 = logic HIGH. (MSB: VID7, LSB: VID0; 11110001b = F1h)

HEX	Voltage	Tolerance	HEX	Voltage	Tolerance	HEX	Voltage	Tolerance	HEX	Voltage	Tolerance
0 0	OFF		4 0	1.21250	+-15mV LL (0 - 110A)	8 0	0.81250	Monotonic	C 0	0.4125	Don't Care
0 1	OFF		4 1	1.20625	+-15mV LL (0 - 110A)	8 1	0.80625	Monotonic	C 1	0.40625	Don't Care
0 2	1.60000	+-15mV LL (0 -	4 2	1.20000	+-15mV LL (0 - 110A)	8 2	0.8	Monotonic	C 2	0.40000	Don't Care
0 3	1.59375	+-15mV LL (0 -	4 3	1.19375	+-15mV LL (0 - 110A)	8 3	0.79375	Monotonic	C 3	0.39375	Don't Care
0 4	1.58750	+-15mV LL (0 -	4 4	1.18750	+-15mV LL (0 - 110A)	8 4	0.7875	Monotonic	C 4	0.38750	Don't Care
0 5	1.58125	+-15mV LL (0 -	4 5	1.18125	+-15mV LL (0 - 110A)	8 5	0.78125	Monotonic	C 5	0.38125	Don't Care
0 6	1.57500	+-15mV LL (0 -	4 6	1.17500	+-15mV LL (0 - 110A)	8 6	0.775	Monotonic	C 6	0.37500	Don't Care
0 7	1.56875	+-15mV LL (0 -	4 7	1.16875	+-15mV LL (0 - 110A)	8 7	0.76875	Monotonic	C 7	0.36875	Don't Care
0 8	1.56250	+-15mV LL (0 -	4 8	1.16250	+-15mV LL (0 - 110A)	8 8	0.7625	Monotonic	C 8	0.36250	Don't Care
0 9	1.55625	+-15mV LL (0 -	4 9	1.15625	+-15mV LL (0 - 110A)	8 9	0.75625	Monotonic	C 9	0.35625	Don't Care
0 A	1.55000	+-15mV LL (0 -	4 A	1.15000	+-15mV LL (0 - 110A)	8 A	0.75	Monotonic	C A	0.35000	Don't Care
0 B	1.54375	+-15mV LL (0 -	4 B	1.14375	+-15mV LL (0 - 110A)	8 B	0.74375	Monotonic	C B	0.34375	Don't Care
0 C	1.53750	+-15mV LL (0 -	4 C	1.13750	+-15mV LL (0 - 110A)	8 C	0.7375	Monotonic	C C	0.33750	Don't Care
0 D	1.53125	+-15mV LL (0 -	4 D	1.13125	+-15mV LL (0 - 110A)	8 D	0.73125	Monotonic	C D	0.33125	Don't Care
0 E	1.52500	+-15mV LL (0 -	4 E	1.12500	+-15mV LL (0 - 110A)	8 E	0.725	Monotonic	C E	0.32500	Don't Care
0 F	1.51875	+-15mV LL (0 -	4 F	1.11875	+-15mV LL (0 - 110A)	8 F	0.71875	Monotonic	C F	0.31875	Don't Care
1 0	1.51250	+-15mV LL (0 -	5 0	1.11250	+-15mV LL (0 - 110A)	9 0	0.7125	Monotonic	D 0	0.31250	Don't Care
1 1	1.50625	+-15mV LL (0 -	5 1	1.10625	+-15mV LL (0 - 110A)	9 1	0.70625	Monotonic	D 1	0.30625	Don't Care
1 2	1.50000	+-15mV LL (0 -	5 2	1.10000	+-15mV LL (0 - 110A)	9 2	0.7	Monotonic	D 2	0.30000	Don't Care
1 3	1.49375	+-15mV LL (0 -	5 3	1.09375	+-15mV LL (0 - 110A)	9 3	0.69375	Monotonic	D 3	0.29375	Don't Care
1 4	1.48750	+-15mV LL (0 -	5 4	1.08750	+-15mV LL (0 - 110A)	9 4	0.6875	Monotonic	D 4	0.28750	Don't Care
1 5	1.48125	+-15mV LL (0 -	5 5	1.08125	+-15mV LL (0 - 110A)	9 5	0.68125	Monotonic	D 5	0.28125	Don't Care
1 6	1.47500	+-15mV LL (0 -	5 6	1.07500	+-15mV LL (0 - 110A)	9 6	0.675	Monotonic	D 6	0.27500	Don't Care
1 7	1.46875	+-15mV LL (0 -	5 7	1.06875	+-15mV LL (0 - 110A)	9 7	0.66875	Monotonic	D 7	0.26875	Don't Care
1 8	1.46250	+-15mV LL (0 -	5 8	1.06250	+-15mV LL (0 - 110A)	9 8	0.6625	Monotonic	D 8	0.26250	Don't Care
1 9	1.45625	+-15mV LL (0 -	5 9	1.05625	+-15mV LL (0 - 110A)	9 9	0.65625	Monotonic	D 9	0.25625	Don't Care
1 A	1.45000	+-15mV LL (0 -	5 A	1.05000	+-15mV LL (0 - 110A)	9 A	0.65	Monotonic	D A	0.25000	Don't Care
1 B	1.44375	+-15mV LL (0 -	5 B	1.04375	+-15mV LL (0 - 110A)	9 B	0.64375	Monotonic	D B	0.24375	Don't Care
1 C	1.43750	+-15mV LL (0 -	5 C	1.03750	+-15mV LL (0 - 110A)	9 C	0.6375	Monotonic	D C	0.23750	Don't Care
1 D	1.43125	+-15mV LL (0 -	5 D	1.03125	+-15mV LL (0 - 110A)	9 D	0.63125	Monotonic	D D	0.23125	Don't Care
1 E	1.42500	+-15mV LL (0 -	5 E	1.02500	+-15mV LL (0 - 110A)	9 E	0.625	Monotonic	D E	0.22500	Don't Care
1 F	1.41875	+-15mV LL (0 -	5 F	1.01875	+-15mV LL (0 - 110A)	9 F	0.61875	Monotonic	D F	0.21875	Don't Care
2 0	1.41250	+-15mV LL (0 -	6 0	1.01250	+-15mV LL (0 - 110A)	A 0	0.6125	Monotonic	E 0	0.21250	Don't Care
2 1	1.40625	+-15mV LL (0 -	6 1	1.00625	+-15mV LL (0 - 110A)	A 1	0.60625	Monotonic	E 1	0.20625	Don't Care
2 2	1.40000	+-15mV LL (0 -	6 2	1.00000	Monotonic DAC (6.25 mV)	A 2	0.6	Monotonic	E 2	0.20000	Don't Care
2 3	1.39375	+-15mV LL (0 -	6 3	0.99375	Monotonic DAC (6.25 mV)	A 3	0.59375	Monotonic	E 3	0.19375	Don't Care
2 4	1.38750	+-15mV LL (0 -	6 4	0.98750	Monotonic DAC (6.25 mV)	A 4	0.5875	Monotonic	E 4	0.18750	Don't Care
2 5	1.38125	+-15mV LL (0 -	6 5	0.98125	Monotonic DAC (6.25 mV)	A 5	0.58125	Monotonic	E 5	0.18125	Don't Care
2 6	1.37500	+-15mV LL (0 -	6 6	0.97500	Monotonic DAC (6.25 mV)	A 6	0.575	Monotonic	E 6	0.17500	Don't Care
2 7	1.36875	+-15mV LL (0 -	6 7	0.96875	Monotonic DAC (6.25 mV)	A 7	0.56875	Monotonic	E 7	0.16875	Don't Care
2 8	1.36250	+-15mV LL (0 -	6 8	0.96250	Monotonic DAC (6.25 mV)	A 8	0.5625	Monotonic	E 8	0.16250	Don't Care
2 9	1.35625	+-15mV LL (0 -	6 9	0.95625	Monotonic DAC (6.25 mV)	A 9	0.55625	Monotonic	E 9	0.15625	Don't Care
2 A	1.35000	+-15mV LL (0 -	6 A	0.95000	Monotonic DAC (6.25 mV)	A A	0.55	Monotonic	E A	0.15000	Don't Care
2 B	1.34375	+-15mV LL (0 -	6 B	0.94375	Monotonic DAC (6.25 mV)	A B	0.54375	Monotonic	E B	0.14375	Don't Care
2 C	1.33750	+-15mV LL (0 -	6 C	0.93750	Monotonic DAC (6.25 mV)	A C	0.5375	Monotonic	E C	0.13750	Don't Care
2 D	1.33125	+-15mV LL (0 -	6 D	0.93125	Monotonic DAC (6.25 mV)	A D	0.53125	Monotonic	E D	0.13125	Don't Care
2 E	1.32500	+-15mV LL (0 -	6 E	0.92500	Monotonic DAC (6.25 mV)	A E	0.525	Monotonic	E E	0.12500	Don't Care
2 F	1.31875	+-15mV LL (0 -	6 F	0.91875	Monotonic DAC (6.25 mV)	A F	0.51875	Monotonic	E F	0.11875	Don't Care
3 0	1.31250	+-15mV LL (0 -	7 0	0.91250	Monotonic DAC (6.25 mV)	B 0	0.5125	Monotonic	F 0	0.11250	Don't Care
3 1	1.30625	+-15mV LL (0 -	7 1	0.90625	Monotonic DAC (6.25 mV)	B 1	0.50625	Monotonic	F 1	0.10625	Don't Care
3 2	1.30000	+-15mV LL (0 -	7 2	0.90000	Monotonic DAC (6.25 mV)	B 2	0.5	Monotonic	F 2	0.10000	Don't Care
3 3	1.29375	+-15mV LL (0 -	7 3	0.89375	Monotonic DAC (6.25 mV)	B 3	0.49375	Don't Care	F 3	0.09375	Don't Care
3 4	1.28750	+-15mV LL (0 -	7 4	0.88750	Monotonic DAC (6.25 mV)	B 4	0.4875	Don't Care	F 4	0.08750	Don't Care
3 5	1.28125	+-15mV LL (0 -	7 5	0.88125	Monotonic DAC (6.25 mV)	B 5	0.48125	Don't Care	F 5	0.08125	Don't Care
3 6	1.27500	+-15mV LL (0 -	7 6	0.87500	Monotonic DAC (6.25 mV)	B 6	0.475	Don't Care	F 6	0.07500	Don't Care
3 7	1.26875	+-15mV LL (0 -	7 7	0.86875	Monotonic DAC (6.25 mV)	B 7	0.46875	Don't Care	F 7	0.06875	Don't Care
3 8	1.26250	+-15mV LL (0 -	7 8	0.86250	Monotonic DAC (6.25 mV)	B 8	0.4625	Don't Care	F 8	0.06250	Don't Care
3 9	1.25625	+-15mV LL (0 -	7 9	0.85625	Monotonic DAC (6.25 mV)	B 9	0.45625	Don't Care	F 9	0.05625	Don't Care
3 A	1.25000	+-15mV LL (0 -	7 A	0.85000	Monotonic DAC (6.25 mV)	B A	0.45	Don't Care	F A	0.05000	Don't Care
3 B	1.24375	+-15mV LL (0 -	7 B	0.84375	Monotonic DAC (6.25 mV)	B B	0.44375	Don't Care	F B	0.04375	Don't Care
3 C	1.23750	+-15mV LL (0 -	7 C	0.83750	Monotonic DAC (6.25 mV)	B C	0.4375	Don't Care	F C	0.03750	Don't Care
3 D	1.23125	+-15mV LL (0 -	7 D	0.83125	Monotonic DAC (6.25 mV)	B D	0.43125	Don't Care	F D	0.03125	Don't Care
3 E	1.22500	+-15mV LL (0 -	7 E	0.82500	Monotonic DAC (6.25 mV)	B E	0.425	Don't Care	F E	OFF	
3 F	1.21875	+-15mV LL (0 -	7 F	0.81875	Monotonic DAC (6.25 mV)	B F	0.41875	Don't Care	F F	OFF	

Typical Applications

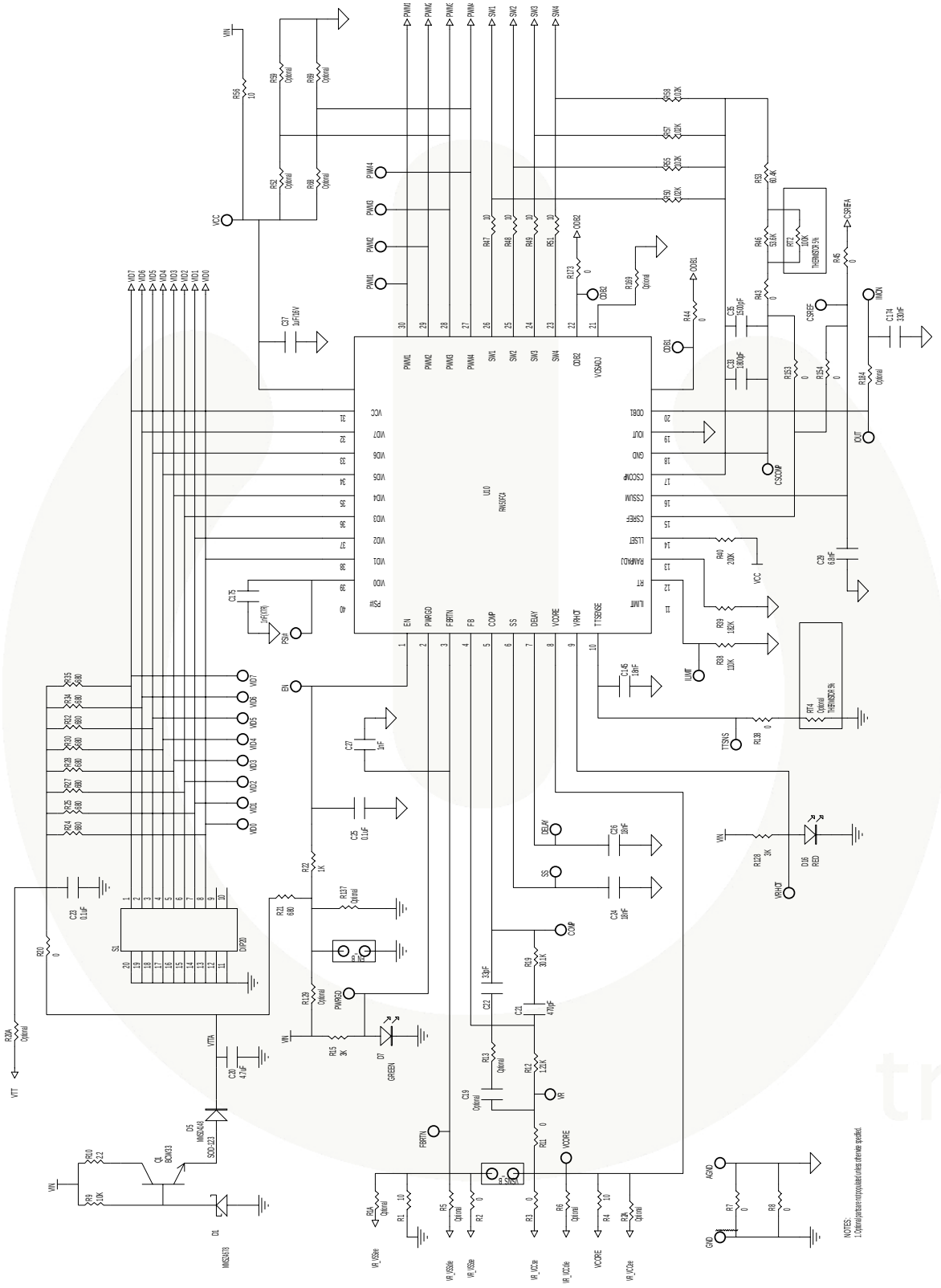


Figure 7. Typical Three-Phase Design, Controller

Note: Contact a Fairchild representative for the latest VR11 reference designs.

Typical Applications (Continued)

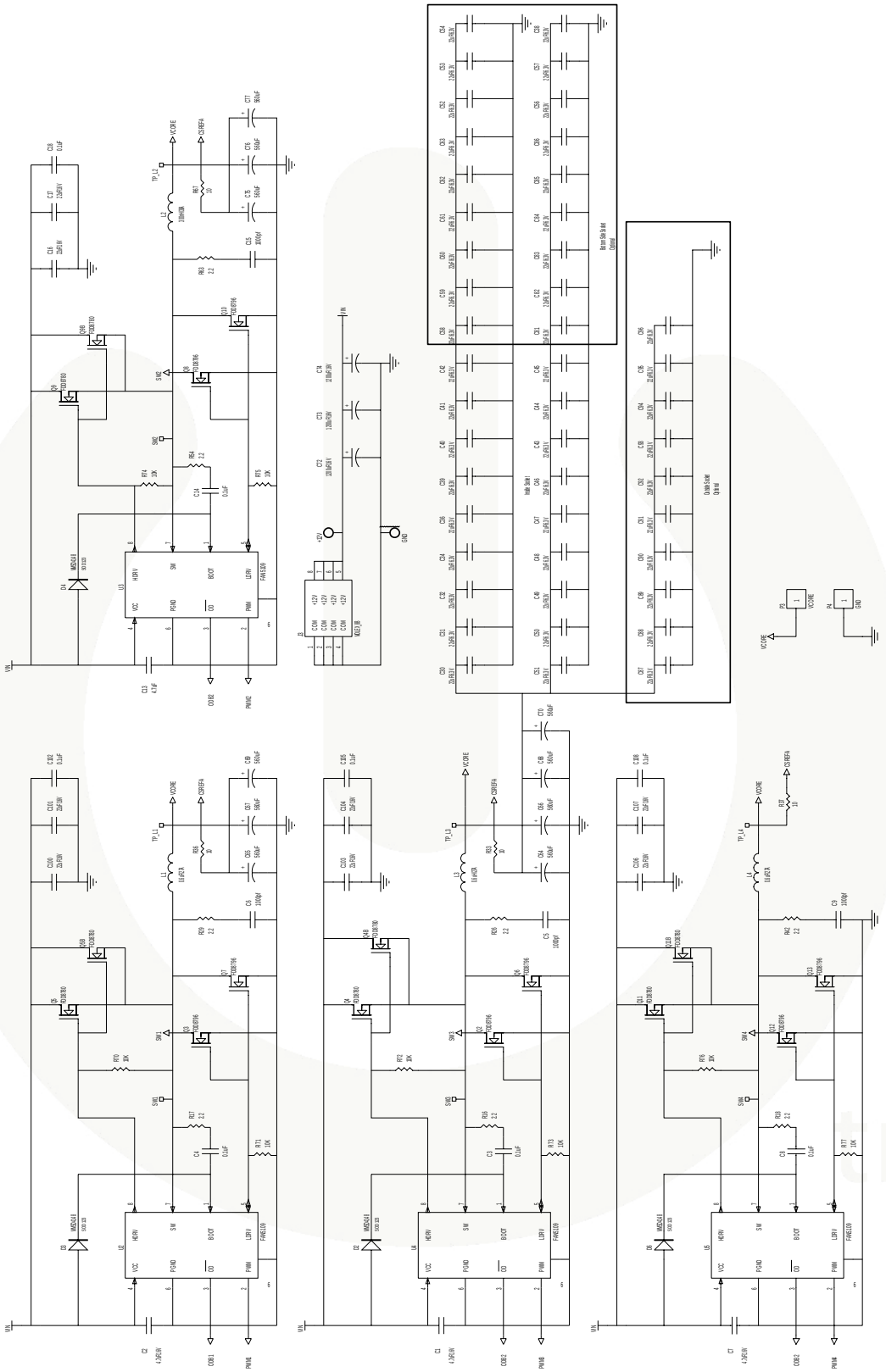


Figure 8. Typical Three-Phase Design, Drivers

Note: Contact a Fairchild representative for the latest VR11 reference designs.

Theory of Operation

Note: The values shown in this section are for reference only. See the parametric tables for actual values.

The FAN50FC3 is a fixed-frequency PWM control with multi-phase logic outputs for use in 2- and 3-phase synchronous buck CPU power supplies. It has an internal VID DAC designed to interface directly with 8-bit VRD/VRM 11 and 7-bit VRD/VRM 10.x compatible CPUs. Multiphase operation is required for the high currents and low voltages of today's microprocessors that can require up to 150A of current.

The integrated features of the FAN50FC3 ensure a stable, high-performance topology for:

- Balanced currents and thermals between phases
- High-speed response at the lowest possible switching frequency and output decoupling capacitors
- Tight load line regulation and accuracy
- High current output by allowing up to 3-phase designs
- Reduced output ripple due to multiphase operation
- Good PC board layout noise immunity
- Easily settable and adjustable design parameters with simple component selection
- 2- to 3-phase operation allows optimizing designs for cost/performance and support a wide range of applications.

Start-Up Sequence

The start-up sequence is shown in Figure 9. Once the EN and UVLO conditions are met, the DELAY pin goes through one cycle (TD1), after which, the internal oscillator starts. The first two clock cycles are used for phase detection. The soft-start ramp is then enabled (TD2), raising the output voltage up to the boot voltage of 1.1V. The boot hold time (TD3) allows the processor VID pins to settle to the programmed VID code. After TD3 timing is finished, the output soft starts, either up or down, to the final VID voltage (during TD4). TD5 is the time between the output reaching the VID voltage and the PWRGD being presented to the system.

Phase-Detection Sequence

During start-up, the number of operational phases and their phase relationship is determined by the internal circuitry that monitors the PWM outputs. Normally, the FAN50FC3 operates as a 3-phase PWM controller. For 2-phase operation, connect the PWM3 pin to V_{CC}.

The PWM logic, which is driven by the master oscillator, directs the phase sequencer and channel detectors. Channel detection is carried out during the first two clock cycles after the chip is enabled. During the detection period, PWM3 is connected to a 100µA sinking current source and two internal voltage comparators check the pin voltage of PWM3 versus a threshold of 3V typical. If the pin is tied to V_{IN}, the pin voltage is above 3V and that phase is disabled and put in a tri-state mode. Otherwise, the internal 100µA current source pulls PWM pin below the 3V threshold. After channel detection, the current source is removed.

Shorting PWM3 to V_{CC} configures the system into 2-phase operation.

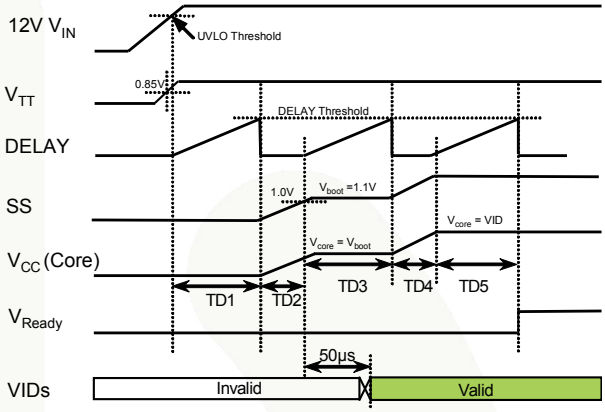


Figure 9. Start-Up Sequence Timing

After detection time is complete, the PWM outputs not sensed as "pulled HIGH" function as normal PWM outputs. PWM outputs sensed as "pulled HIGH" are put into a high-impedance state.

The PWM signals are logic-level outputs intended for driving external gate drivers, such as the FAN5109. Since each phase is monitored independently; operation approaching 100% duty cycle is possible. More than one output can be on at the same time to allow phase overlap.

Master Clock Frequency

The clock frequency is set with an external resistor connected from the RT pin to ground. The frequency-to-resistor relationship is shown in the graph in Figure 6. To determine the frequency per phase, divide the clock by the number of enabled phases.

Output Current Sensing

The FAN50FC3 provides a dedicated current-sense amplifier (CSA) to monitor the output current for proper voltage positioning and for current limit detection *(see Figure 1)*. It differentially senses the voltage drop across the DCR of the inductors to give the total average current being delivered to the load. This method is inherently more accurate than peak current detection or sampling the voltage across the low-side MOSFETs. The CSA implementation can be configured for the objectives of the system. It can use output inductor DCR sensing without a thermistor for lowest cost or output inductor DCR sensing with a thermistor for improved accuracy with tracking of inductor temperature.

To measure the differential voltage across the output inductors, the positive input of the CSA (CSREF pin) is connected, using equal value resistors, to the output capacitor side of the inductors. The negative input of the CSA (CSSUM pin) is connected, using equal value resistors, to the MOSFET side of the inductors. The CSA's output (CSCOMP) is a voltage equal to the voltage dropped across the inductors, times the gain of the CSA, and is inversely proportional to the output current.

The gain of the CSA is set by connecting an external feedback resistor between the CSA's CSCOMP and CSSUM pins. A capacitor, connected across the resistor, is used to create a low-pass filter to remove high frequency switching effects and create a RC pole to cancel the zero created by the L/DCR of the inductor. The end result is that the voltage between the CSCOMP and CSREF pins is inversely proportional to the output current (CSCOMP goes negative relative to CSREF as current increases) and the CSA gain sets the ratio of the CSA output voltage change as a function of output current change. This difference in voltage is used by the current limit comparator and by the droop amplifier to create the output load line.

The CSA is designed to have a low offset input voltage. The sensing gain is determined by external resistors, so it can be made extremely accurate.

Load Line Impedance Control

The FAN50FC3 has an internal "Droop Amp" that effectively subtracts the voltage applied between the CSCOMP and CSREF pins from the FB pin voltage of the error amplifier, allowing the output voltage to be varied independent of the DAC setting. A positive voltage on CSCOMP (relative to CSREF) increases the output voltage and a negative voltage decreases it. Since the voltage between the CSA's CSCOMP and CSREF pins is inversely proportional to the output, current causes the output voltage to decrease an amount directly proportional to the increase in output current creating a droop or load line. The ratio of output voltage decrease to output current increase is the effective R_o of the power supply and is set by the DC gain of the CSA.

Current Control Mode & Thermal Balance

The FAN50FC3 has individual SW inputs for each phase. They are used to measure the voltage drop across the bottom FETs to determine the current in each phase. This information is combined with an internal ramp to create a current balancing feedback system. This gives good current balance accuracy that takes into account, not only the current, but also the thermal balance between the bottom FETs in each phase.

External resistors R_{SW1} through R_{SW3} can be placed in series with individual SW inputs to create an intentional current imbalance, such as in cases where one phase may have better cooling and can support higher currents. It is best to have the ability to add these resistors in the initial design, to ensure that placeholders are provided in the layout. To increase the current in a phase, increase R_{SW} for that phase. Adding a resistor of a few hundred ohms can make a noticeable increase in current, so use small steps.

The amplitude of the internal ramp is set by a resistor connected between the input voltage and the RAMPADJ pin. This method also implements the voltage feedforward function.

Output Voltage Differential Sensing

The FAN50FC3 uses differential sensing in conjunction with a high-accuracy DAC and a low-offset error amplifier to maintain a worst-case specification of ±7.7mV differential sensing accuracy over its specified operating range.

A high gain-bandwidth error amplifier is used for the voltage control loop. The voltage on the FB pin is compared to the DAC voltage to control the output voltage. The FB voltage is also effectively offset by the CSA output voltage for accurately positioning the output voltage as a function of current. The output of the error amplifier is the COMP pin, which is compared to the internal PWM ramps to create the PWM pulse widths.

The negative input (FB) is tied to the output sense location with a resistor R_B and is used for sensing and controlling the output voltage at this point. Additionally a current source is connected internally to the FB pin, which causes a fixed DC current to flow through R_B. This current creates a fixed voltage drop (offset voltage) across R_B. The offset voltage adds to the sensed output voltage, which causes the error amplifier to regulate the actual output voltage lower than the programmed VID voltage by this amount. The main loop compensation is incorporated into the feedback by an external network connected between FB and COMP.

Delay Timer

The delay times for the start-up timing sequence are set with a capacitor from the DELAY pin to ground, as stated in the Start-Up Sequence section. In UVLO or when EN is logic LOW, the DELAY pin is held at ground. Once the UVLO and EN are asserted, a 15µA current flows out of the DELAY pin to charge C_{DLY}. A comparator, with a threshold of 1.7V, monitors the DELAY pin voltage. The delay time is therefore set by the 15µA charging the delay capacitor from 0V to 1.7V. This DELAY pin is used for multiple delay timings (TD1, TD3, and TD5) during start-up. DELAY is also used for timing the current-limit latch-off, as explained in the *Current Limit* section.

Soft-Start

The soft-start times for the output voltage are set with a capacitor from the SS pin to ground. After TD1 and the phase-detection cycle are complete, the SS time (TD2 in Figure 9) starts. The SS pin is disconnected from GND and the capacitor is charged up to the 1.1V boot voltage by the SS amplifier, which has a limited output current of 15µA. The voltage at the FB pin follows the ramping voltage on the SS pin, limiting the inrush current during start-up. The soft-start time depends on the value of the boot voltage and C_{SS}.

Once the SS voltage is within 100mV of the boot voltage, the boot voltage delay time (TD3) is started. The end of the boot voltage delay time signals the beginning of the second soft-start time (TD4). The SS voltage changes from the boot voltage to the programmed VID DAC voltage (either higher or lower) using the SS amplifier with the limited output current of 15µA. The voltage of the FB pin follows the ramping voltage of the SS pin, limiting the inrush current during the transition from the boot voltage to the final DAC voltage. The second soft-start time depends on the boot voltage, the programmed VID DAC voltage, and C_{SS}.

If either EN is taken LOW or V_{CC} drops below UVLO, DELAY and SS are reset to ground to be ready for another soft-start cycle. Figure 10 shows typical start-up waveforms for the FAN50FC3.

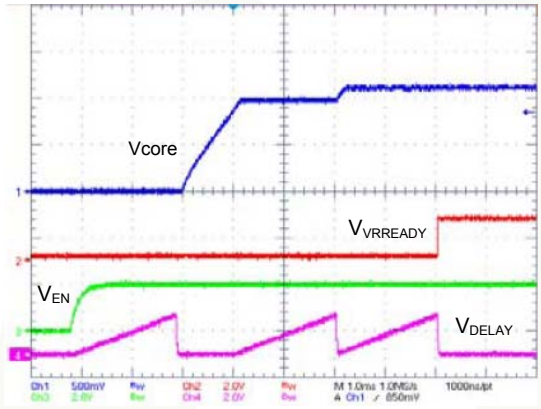


Figure 10. Start-up Waveforms

Current-Limit, Short-Circuit, and Latch-Off Protections

The FAN50FC3 compares a programmable current-limit set point to the voltage from the output of the current sense amplifier. The current-limit level is set with the resistor from the ILIMIT pin to ground. During operation, the voltage on ILIMIT is 1.7V. The current through the external resistor is internally scaled to give a current limit threshold of 10mV/µA. If the voltage between CSREF and CSCOMP rises above the current-limit threshold, the internal current-limit amplifier controls the internal COMP voltage to maintain the average output current at the limit.

After TD5 has completed, an over-current (OC) event starts a latch-off delay timer. The delay timer uses the DELAY pin timing capacitor. During current limit, the DELAY pin current is reduced to 3.75µA. When the voltage on the delay pin reaches 1.7V, the controller shuts down and latches off. The current limit latch-off delay time is therefore set by the current of 3.75µA charging the delay capacitor 1.7V. This delay is four times longer than the delay time during the start-up sequence. If there is a current limit during start-up, the FAN50FC3 goes through TD1 to TD5 in current limit, then starts the latch-off timer. Because the controller continues to operate during the latch-off delay time, if the OC is removed before the 1.7V threshold is reached, the controller returns to normal operation and the DELAY capacitor is reset to GND.

The latch-off function can be reset by cycling the supply voltage to the FAN50FC3 or by toggling the EN pin LOW for a short time. To disable the short-circuit latch-off function, an external resistor can be placed in parallel with C_{DLY} to prevent the DELAY capacitor from charging up to the 1.7V threshold. The addition of this resistor causes a slight increase in the delay times.

During start-up, when the output voltage is below 200mV, a secondary current limit is active. This secondary current limit clamps the internal COMP voltage at the PWM comparators to 1.5V. Typical over-current latch-off waveforms are shown in Figure 11.

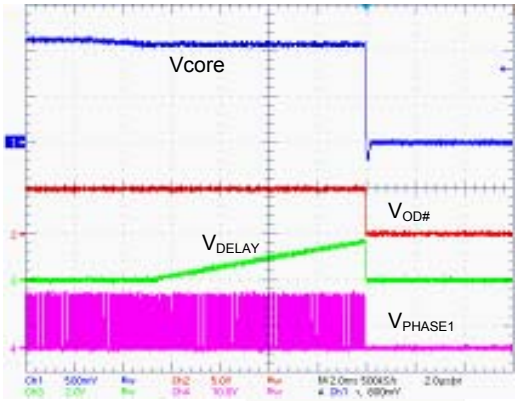


Figure 11. Over-Current Latch-off Waveforms

FastvCore™ Operation

FastvCore™ improves the transient response for a load step-up change. Normally a controller has to wait till the next clock cycle if a load step-up happens during between PWM signals. With FastvCore™, the controller is able to immediately respond to the load step change, so that the inductor current increases to the new load current in a shorter period of time.

FastvCore™ is adjusted by connecting a resistor (R_{SETOS}) between pin 16 (VOSADJ) and AGND to set the threshold where FastvCore™ is initiated.

$$R_{SETOS} = (V_{OS}+LLTOB) \bullet R_T \bullet 10 \qquad \text{EQ. 1}$$

where:

R_T = the frequency set resistor

V_{OS} = the target FastvCore™ detection threshold that is the voltage difference between the output voltage starting point and the voltage when the FastvCore™ starts to respond to a load step-up change

LLTOB= the socket load line tolerance band

FastvCore™ design example:

If:

R_T = 267kohm
V_{OS} = 35mV
LLTOB = +/-19mV

Then:

R_{SETOS} = $(V_{OS}+LLTOB) \bullet R_T \bullet 10$
= $(35mV+19mV) \bullet 267kohm \bullet 10$
= 144.2kohm

Dynamic VID

The FAN50FC3 has the ability to dynamically change the VID inputs while the controller is running. This allows the output voltage to change while the supply is running and supplying current to the load. This is commonly referred to as VID on-the-fly (OTF). A VID OTF can occur under light or heavy load conditions. The processor signals the controller by changing the VID inputs in multiple steps from the start code to the finish code. This change can be positive or negative.

When a VID input changes state, the FAN50FC3 detects the change and ignores the DAC inputs for a minimum of 200ns. This time prevents a false code due to logic skew while the eight VID inputs are changing. Additionally, the first VID change initiates the PWRGD and CROWBAR blanking functions for a minimum of 100µs to prevent a false PWRGD or CROWBAR event. Each VID change resets the internal timer.

Power Good Monitoring

The power good comparator monitors the output voltage via the CSREF pin. The PWRGD pin is an open-drain output whose high level (when connected to a pull-up resistor) indicates that the output voltage is within the nominal limits specified based on the VID voltage setting. PWRGD goes low if the output voltage is outside of this specified range, if the VID DAC inputs are in no CPU mode, or whenever the EN pin is pulled low. PWRGD is blanked during a VID OTF event for a period of ~200µs to prevent false signals during the time the output is changing.

The PWRGD circuitry also incorporates an initial turn-on delay time (TD5) based on the DELAY timer. Prior to the SS voltage reaching the programmed VID DAC voltage, 100mV, the PWRGD pin is held low. Once the SS pin is within 100mV of the programmed DAC voltage, the capacitor on the DELAY pin begins to charge up. A comparator monitors the DELAY voltage and enables PWRGD when the voltage reaches 1.7V. The PWRGD delay time is therefore set by a current of 15µA charging a capacitor from 0V to 1.7V.

Output Crowbar

As part of the protection for the load and output components of the supply, the PWM outputs are driven low (turning on the low-side MOSFETs) when the output voltage exceeds the upper crowbar threshold. This crowbar action stops once the output voltage falls below the release threshold of approximately 300mV.

Turning on the low-side MOSFETs pulls down the output as the reverse current builds up in the inductors. If the output over-voltage is due to a short in the high-side MOSFET, this action current-limits the input supply, protecting the microprocessor.

Output Enable and UVLO

For the FAN50FC3 to begin switching, the input supply (V_{CC}) to the controller must be higher than the UVLO threshold and the EN pin must be higher than its 0.85V threshold. This initiates a system start-up sequence. If either UVLO or EN is less than their respective thresholds, the FAN50FC3 is disabled; which holds the PWM outputs low, discharges the DELAY and SS capacitors, and forces PWRGD and OD# signals low.

In the application circuit, the OD# pin should be connected to the OD# inputs of the FAN5009 or FAN5109 drivers. Pulling OD# LOW disables the drivers such that both DRVH and DRVL are driven low. This turns off the bottom MOSFETs to prevent them from discharging the output capacitors through the output inductors. If the bottom MOSFETs were left on, the output capacitors could ring with the output inductors and produce a negative output voltage to the processor.

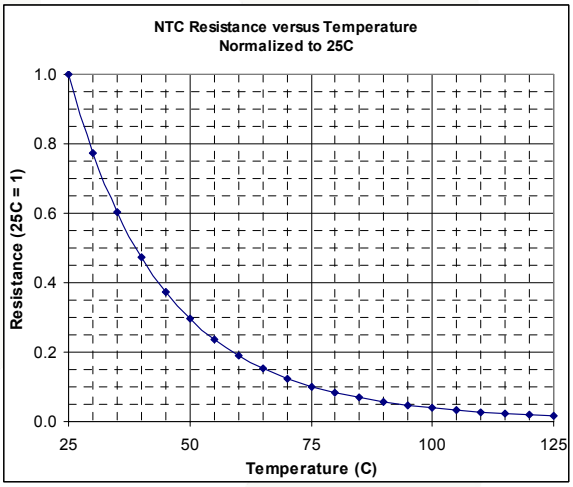


Figure 12. Typical NTC Resistance vs. Temperature

Applications and Component Selection

Please consult Fairchild Application Note:

AN-6052 — Instructions for the Multi-Phase VR11 MathCad® Design Tool

Layout and Component Placement

The following guidelines are recommended for optimal performance of a switching regulator in a PC system.

General Recommendations

For good results, a PCB with at least four layers is recommended. This should allow the needed versatility for control circuitry interconnections with optimal placement, power planes for ground, input and output power, and wide interconnection traces in the remainder of the power delivery current paths. Keep in mind that each square unit of one-ounce copper trace has a resistance of ~0.53mΩ at room temperature.

Whenever high currents must be routed between PCB layers, vias should be used liberally to create several parallel current paths so that the resistance and inductance introduced by these current paths is minimized and the via current rating is not exceeded.

If critical signal lines (including the output voltage sense lines of the FAN50FC3) must cross through power circuitry, it is best if a signal ground plane can be interposed between those signal lines and the traces of the power circuitry. This serves as a shield to minimize noise injection into the signals at the expense of making signal ground a bit noisier.

An analog ground plane should be around and under the FAN50FC3 as a reference for the components associated with the controller. This plane should be tied to the nearest output decoupling capacitor ground and should not be tied to any other power circuitry to prevent power currents from flowing in it.

The components around the FAN50FC3 should be located close to the controller with short traces. The most important traces to keep short and away from other traces are the FB and CSSUM pins. The output capacitors should be connected as close as possible to the load (or connector); for example, a microprocessor core that receives the power. If the load is distributed, the capacitors should be distributed and generally be in proportion to where the load tends to be more dynamic.

Avoid crossing any signal lines over the switching power path loop described in the following section.

Power Circuitry Recommendations

The switching power path should be routed on the PCB to encompass the shortest possible length to minimize radiated switching noise energy (i.e., EMI) and conduction losses in the board. Failure to take proper precautions can result in EMI problems for the entire PC system as well as noise-related operational problems in the power converter control circuitry. The switching power path is the loop formed by the current path through the input capacitors and the power MOSFETs, including all interconnecting PCB traces and planes. Using short and wide interconnection traces is especially critical in this path for two reasons: it minimizes the inductance in the switching loop, which can cause high energy ringing, and it accommodates the high-current demand with minimal voltage loss.

Whenever a power dissipating component, for example, a power MOSFET, is soldered to a PCB, the liberal use of vias, both directly on the mounting pad and immediately surrounding it, is recommended. Two important reasons for this are improved current rating through the vias and improved thermal performance from vias extended to the opposite side of the PCB, where a plane can more readily transfer the heat to the air. Make a mirror image of any pad being used to heatsink the MOSFETs on the opposite side of the PCB to achieve the best thermal dissipation to the air around the board. To further improve thermal performance, use the largest possible pad area.

The output power path should also be routed to encompass a short distance. The output power path is formed by the current path through the inductor, the output capacitors, and the load.

For best EMI containment, a solid power ground plane should be used as one of the inner layers, extending fully under all the power components.

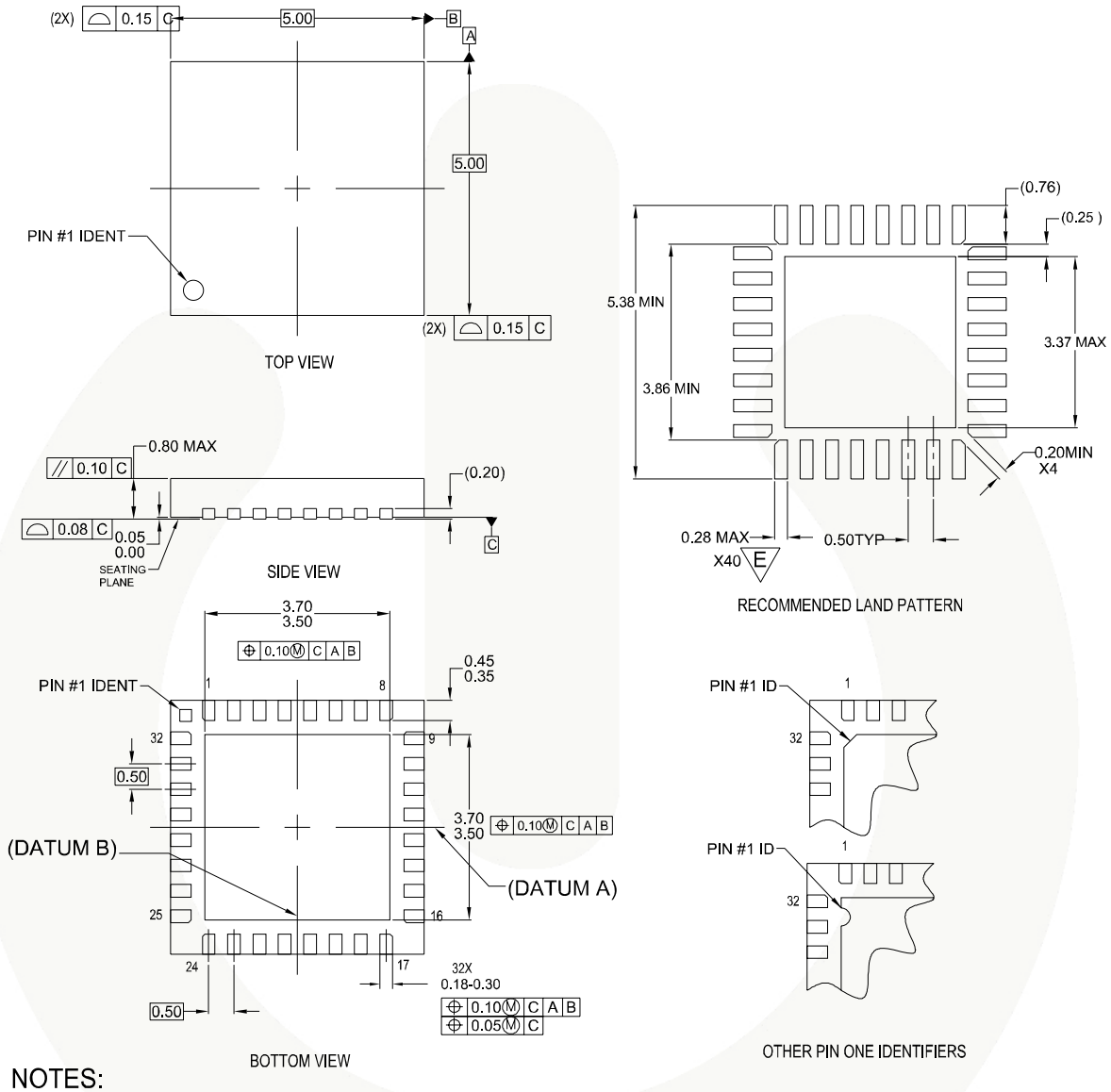
Signal Circuitry Recommendations

The output voltage is sensed and regulated between the FB pin and the FBRTN pin, which connect to the signal ground at the load. To avoid differential mode noise pickup in the sensed signal, the loop area should be small. Thus, the FB and FBRTN traces should be routed adjacent to each other on top of the power ground plane back to the controller.

The feedback traces from the switch nodes should be connected as close as possible to the inductor. The CSREF signal should be connected to the output voltage at the nearest inductor to the controller.

Physical Dimensions

Dimensions are in millimeters (inches) unless otherwise noted.



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-220, VARIATION WHHD-4
THIS PACKAGE IS ALSO FOOTPRINT COMPATIBLE WITH WHHD-5

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994

D. LAND PATTERN PER IPC SM-782 FABRICATION AND ASSEMBLY TOLERANCES OF 0.1 MM APPLIED

E. WIDTH REDUCED TO AVOID SOLDER BRIDGING.

G. DIMENSIONS ARE NOT INCLUSIVE OF BURRS,
MOLD FLASH, NOR TIE BAR PROTRUSIONS.

MLP032ArevB

Figure 13. 32-Pin, Molded Leadless Package (MLP), JEDEC MO-220, 5mm Square

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